Fig.1

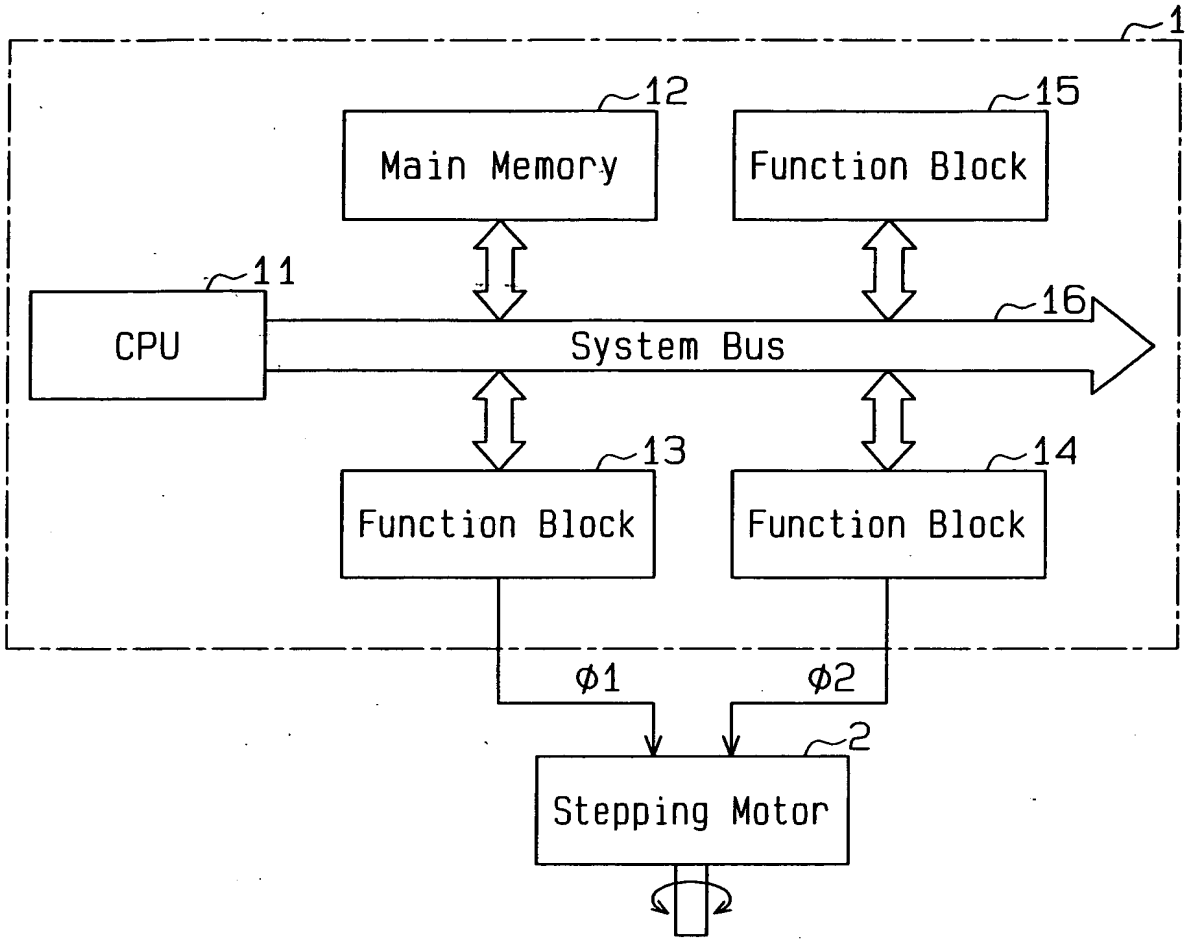
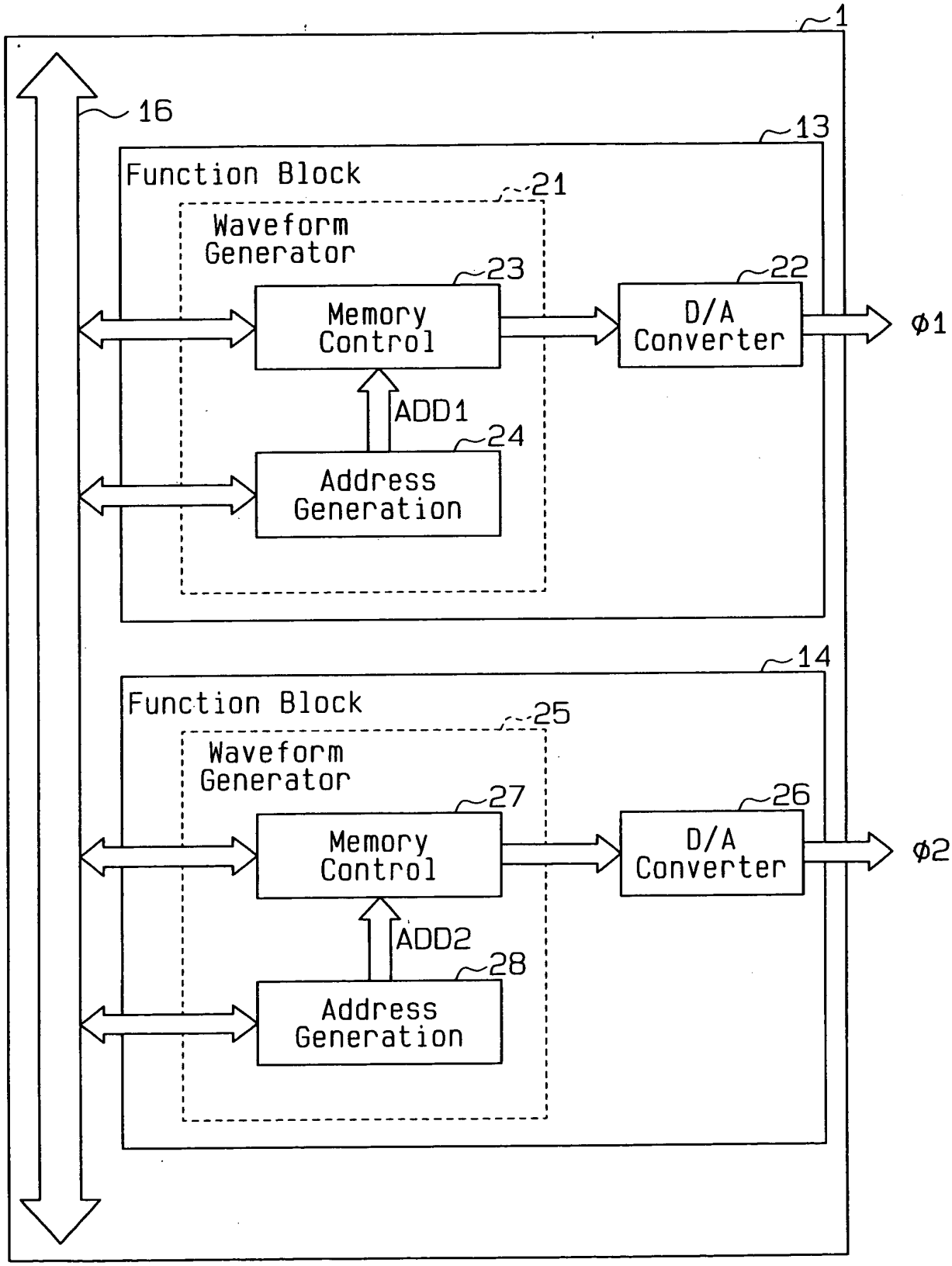

1
12
Main Memory
15
Function Block
11
CPU
16
System Bus
13
Function Block
14
Function Block
φ1
φ2
2
Stepping Motor

Fig.2


1
16
13
Function Block
21
Waveform Generator
23
Memory Control
22
D/A Converter
φ1
ADD1
24
Address Generation
14
Function Block
25
Waveform Generator
27
Memory Control
26
D/A Converter
φ2
ADD2
28
Address Generation

DOCID: EP 0 813 136 A2

Fig.3

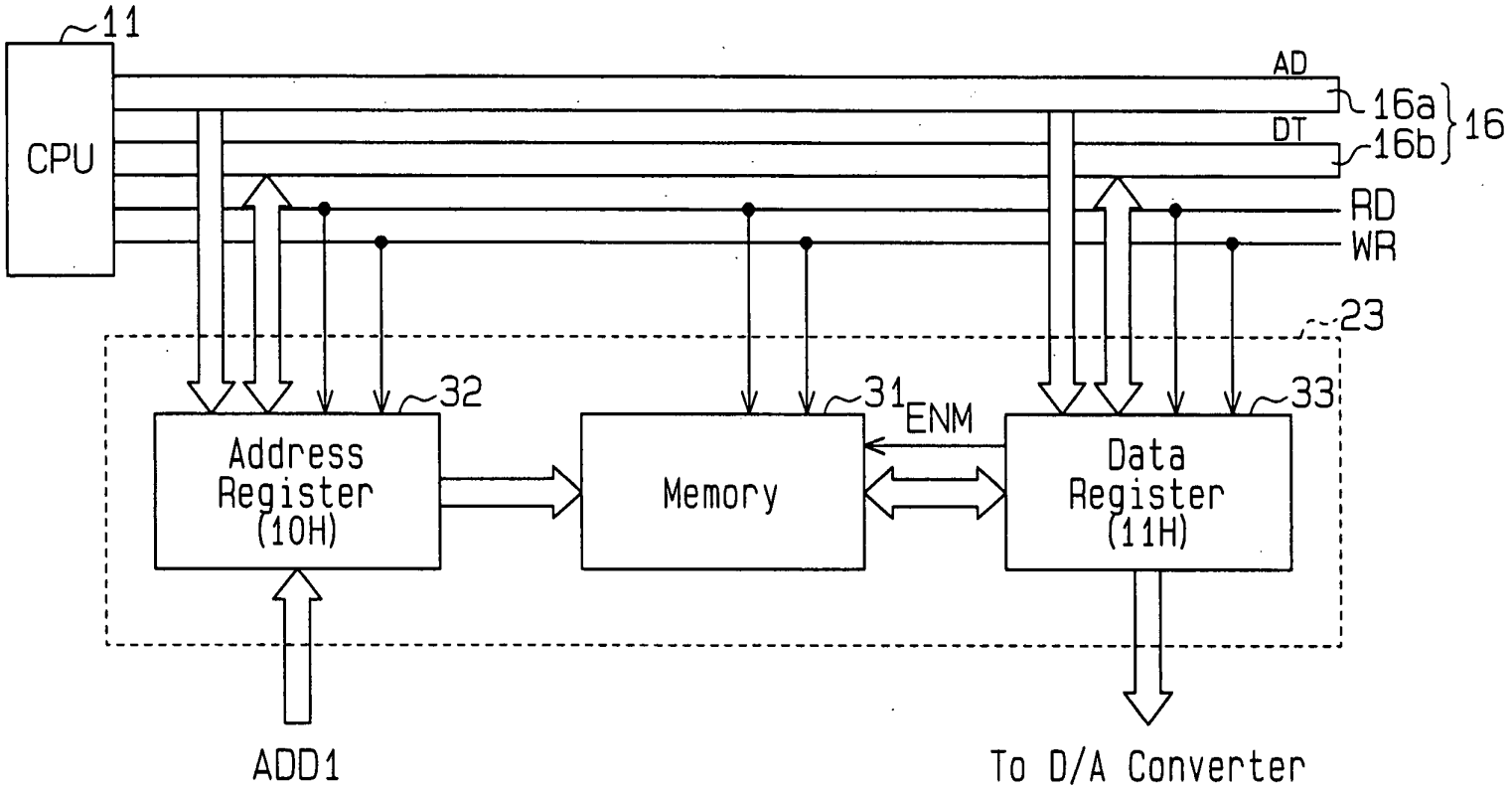


Fig.4

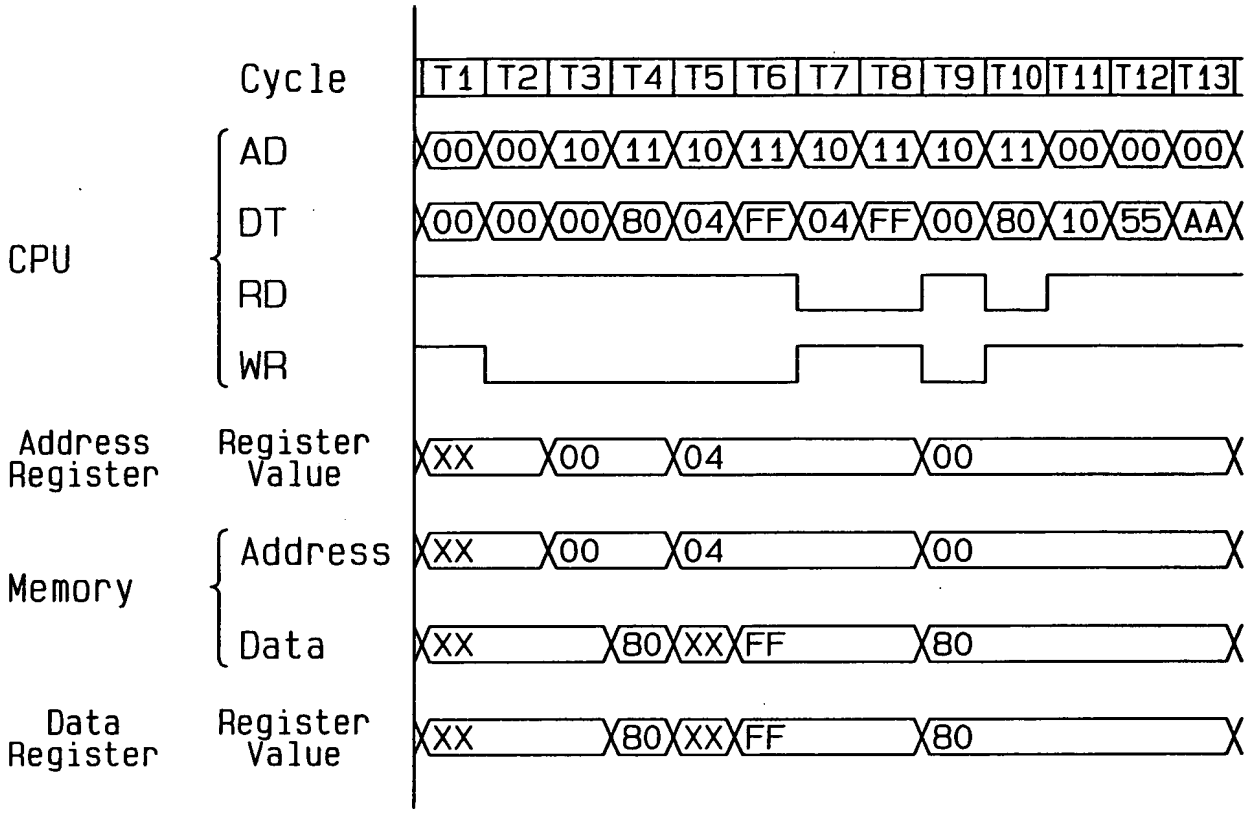

Cycle
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
CPU
AD
00 00 10 11 10 11 10 11 10 11 00 00 00
DT
00 00 00 80 04 FF 04 FF 00 80 10 55 AA
RD
WR
Address Register
Register Value
XX 00 04 00
Memory
Address
XX 00 04 00
Data
XX 80 XX FF 80
Data Register
Register Value
XX 80 XX FF 80

Fig.5

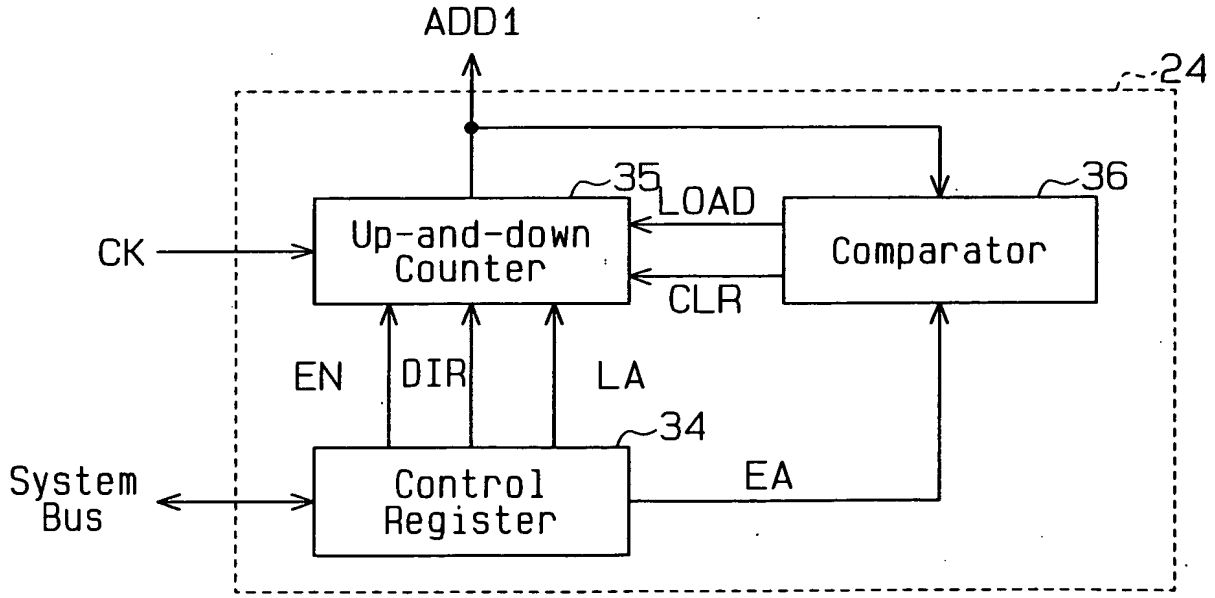

ADD1
24
35
LOAD
36
CK
Up-and-down Counter
Comparator
CLR
EN
DIR
LA
34
System Bus
Control Register
EA

Fig.6

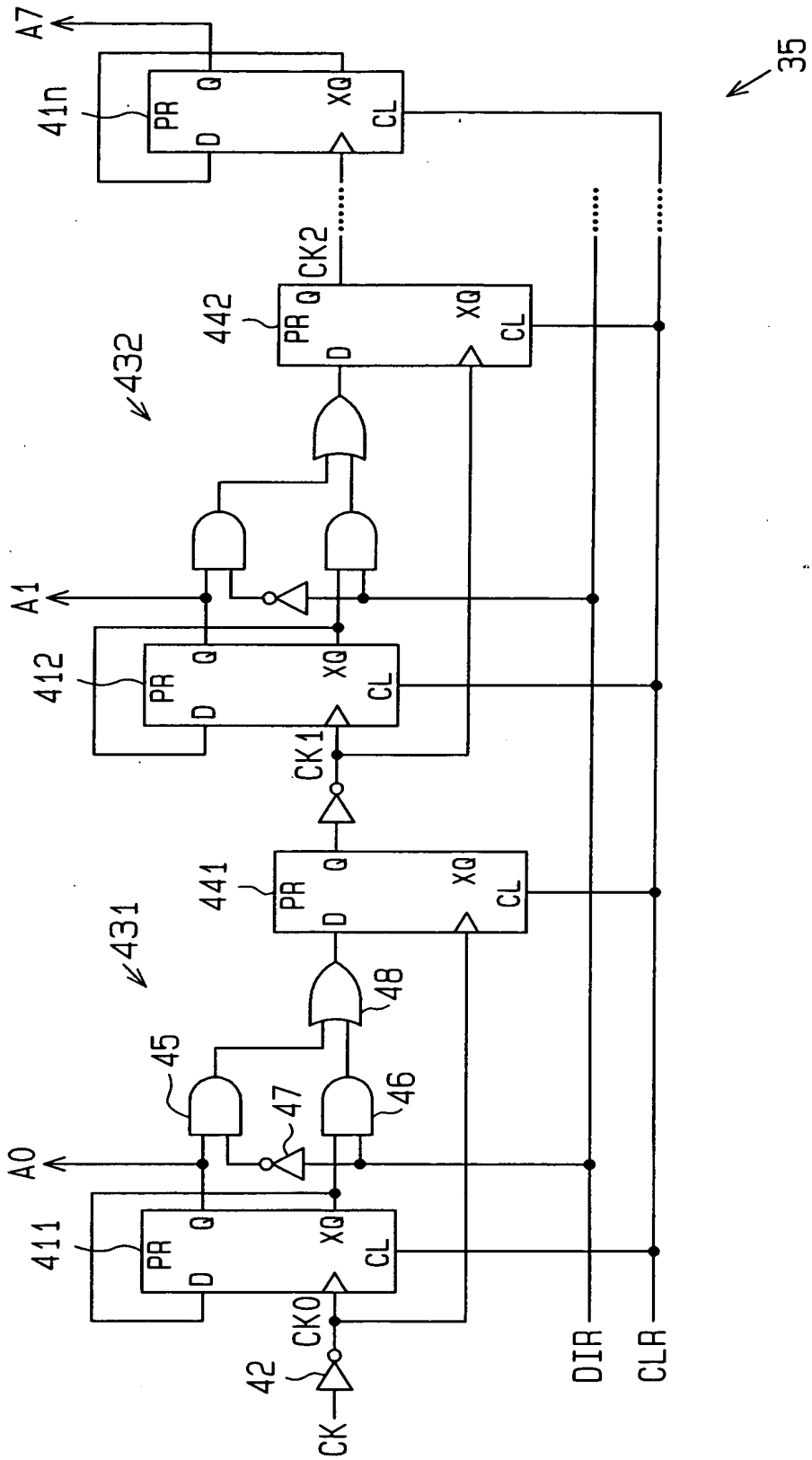

A7
41n
PR
D
Q
XQ
CL
35
CK2
442
432
A1
412
CK1
441
431
48
45
47
46
A0
411
CK0
42
CK
DIR
CLR

Fig.7

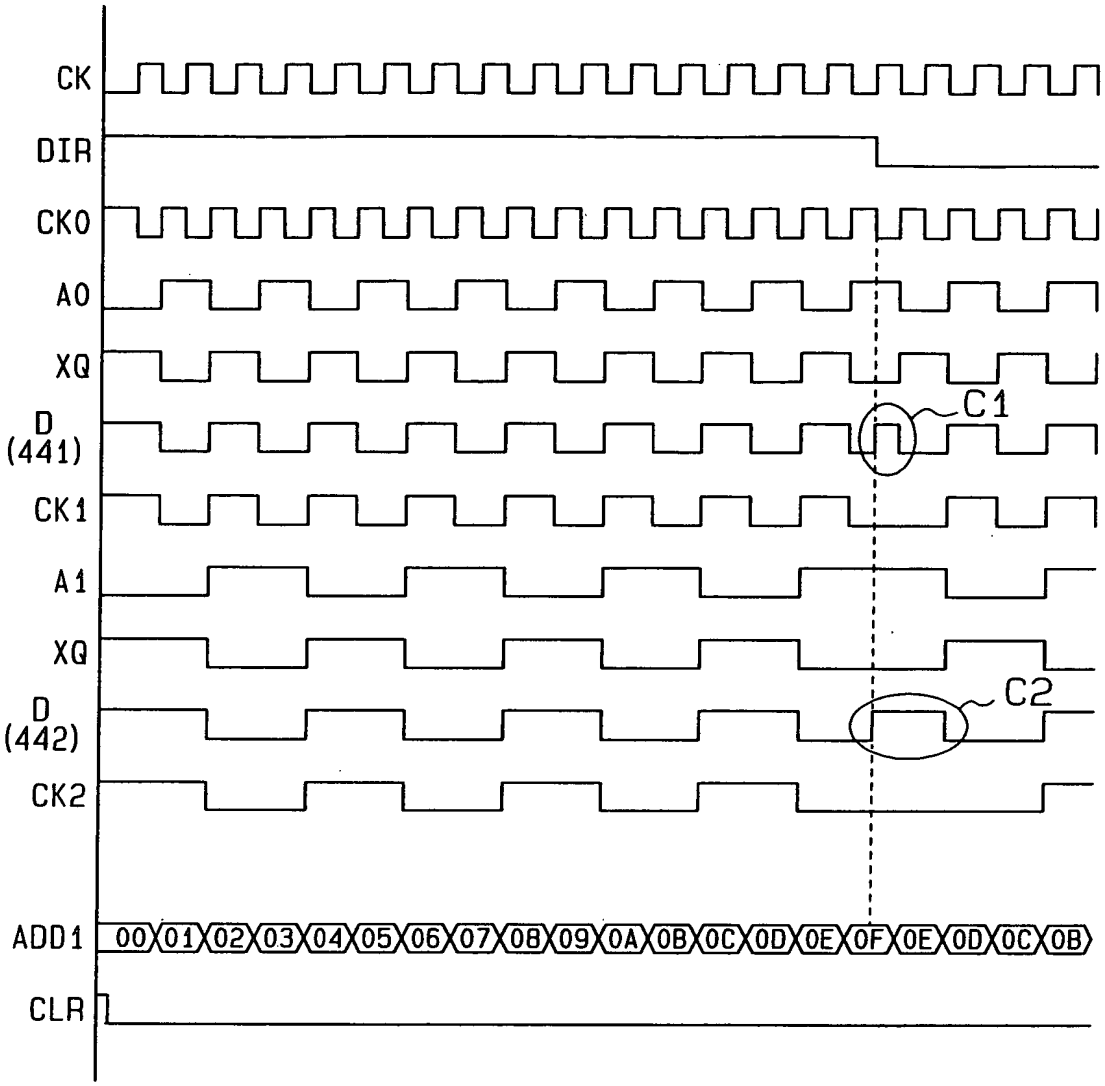

CK
DIR
CKO
AO
XQ
D
(441)
C1
CK1
A1
XQ
D
(442)
C2
CK2
ADD1
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 0E 0D 0C 0B
CLR

Fig.8

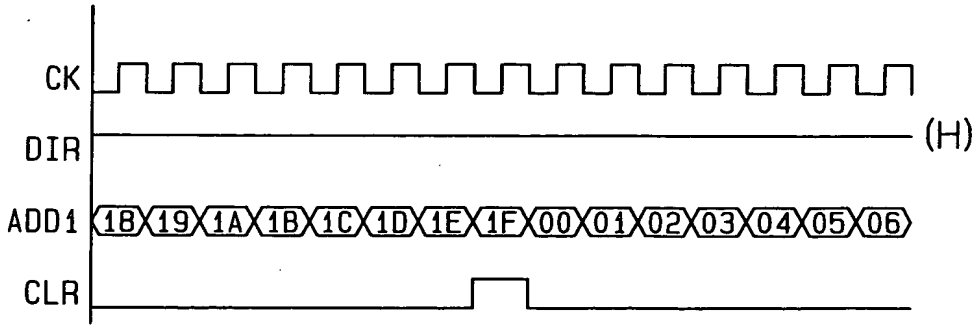

CK
DIR
(H)
ADD1
18 19 1A 1B 1C 1D 1E 1F 00 01 02 03 04 05 06
CLR

Fig.9

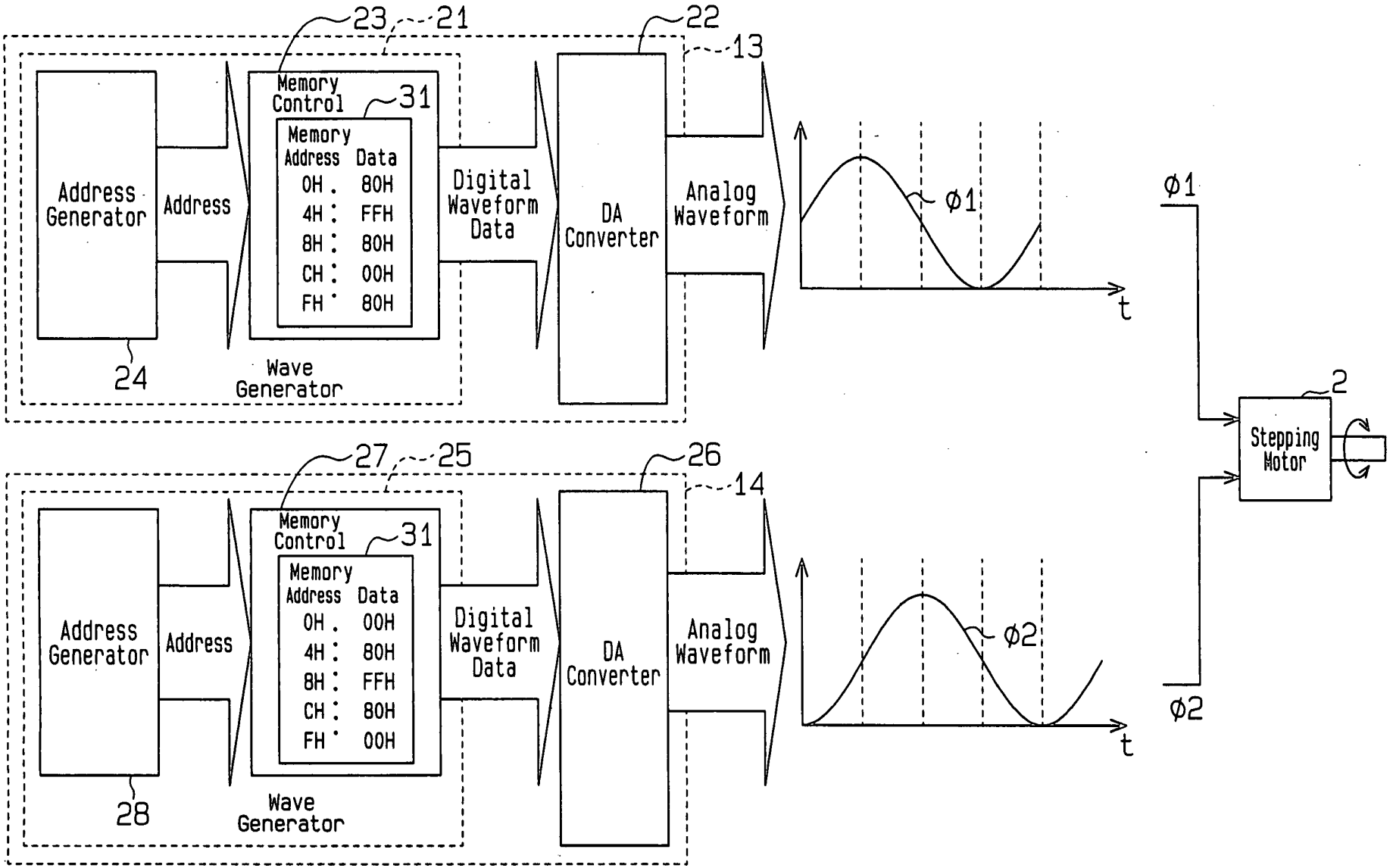

23
21
22
13
Memory Control
31
Memory
Address Data
0H . 80H
4H : FFH
8H : 80H
CH : 00H
FH . 80H
Address Generator
Address
Digital Waveform Data
DA Converter
Analog Waveform
φ1
t
24
Wave Generator
φ1
2
Stepping Motor
27
25
26
14
Memory Control
31
Memory
Address Data
0H . 00H
4H : 80H
8H : FFH
CH : 80H
FH . 00H
Address Generator
Address
Digital Waveform Data
DA Converter
Analog Waveform
φ2
t
28
Wave Generator
φ2

Fig.10

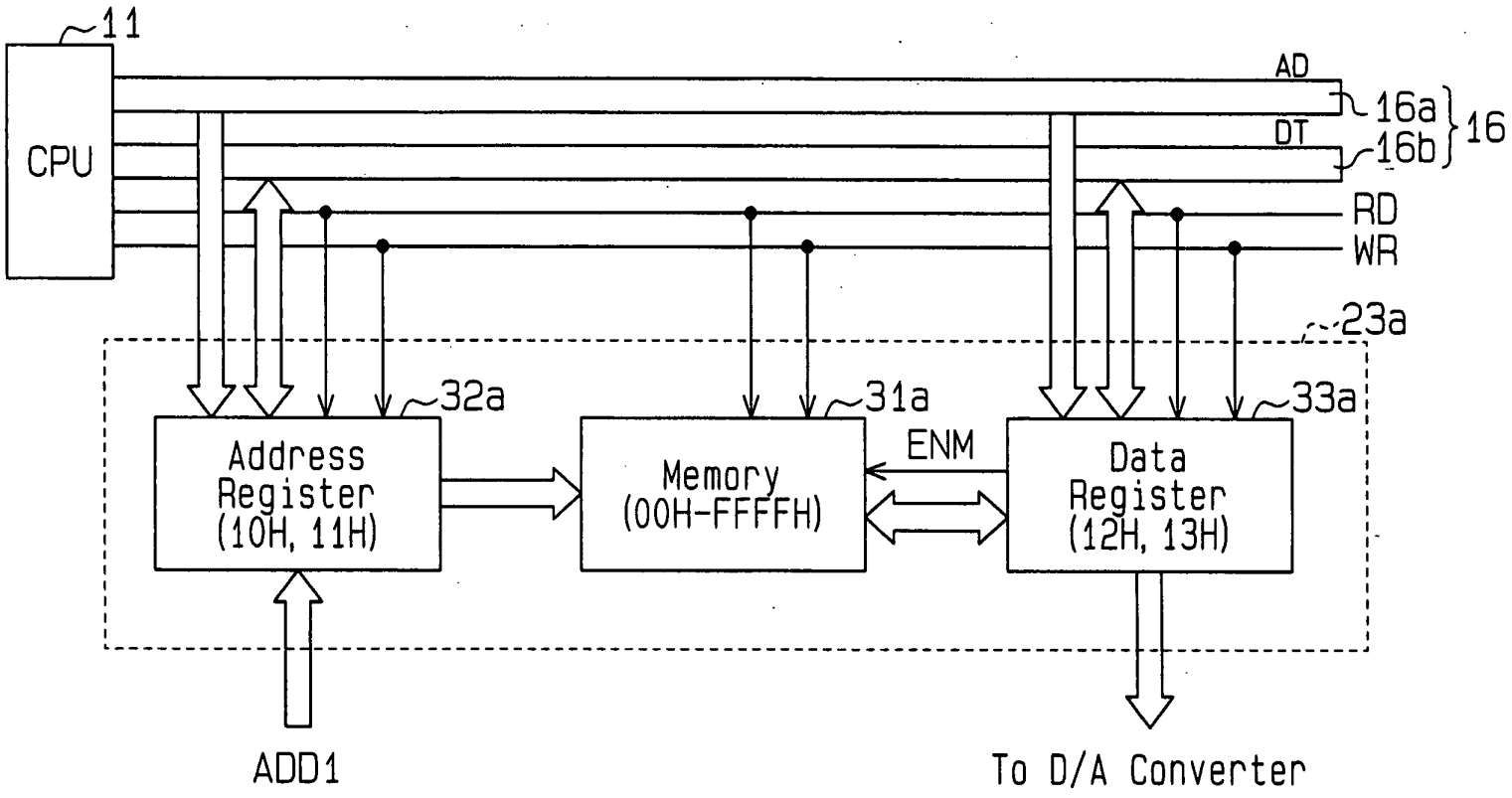

11
CPU
AD
16a
DT
16b
16
RD
WR
23a
32a
31a
33a
Address Register (10H, 11H)
Memory (00H-FFFFH)
ENM
Data Register (12H, 13H)
ADD1
To D/A Converter

Fig.11

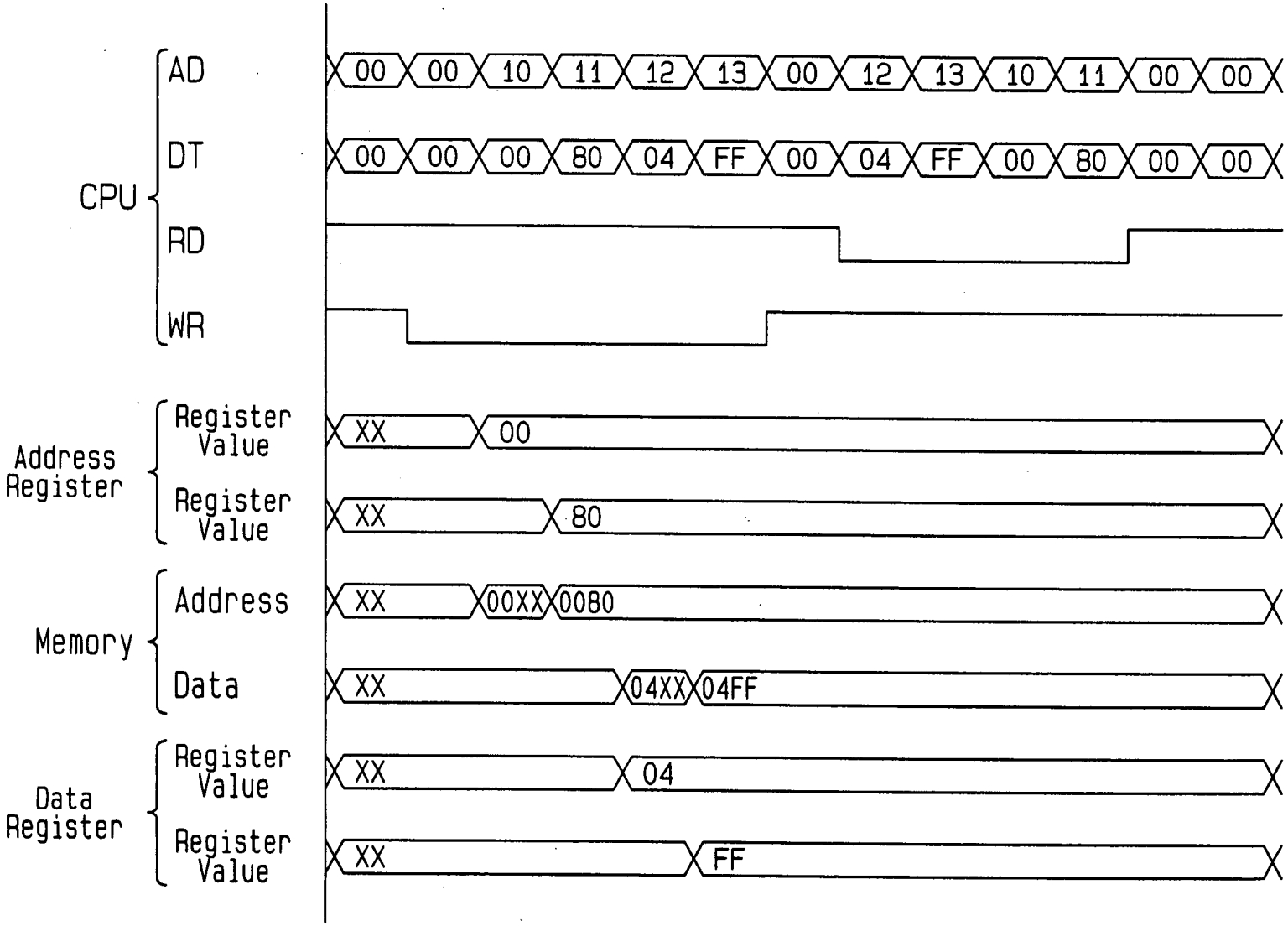

CPU
AD
00 00 10 11 12 13 00 12 13 10 11 00 00
DT
00 00 00 80 04 FF 00 04 FF 00 80 00 00
RD
WR
Address Register
Register Value
XX 00
Register Value
XX 80
Memory
Address
XX 00XX 0080
Data
XX 04XX 04FF
Data Register
Register Value
XX 04
Register Value
XX FF

Fig.12

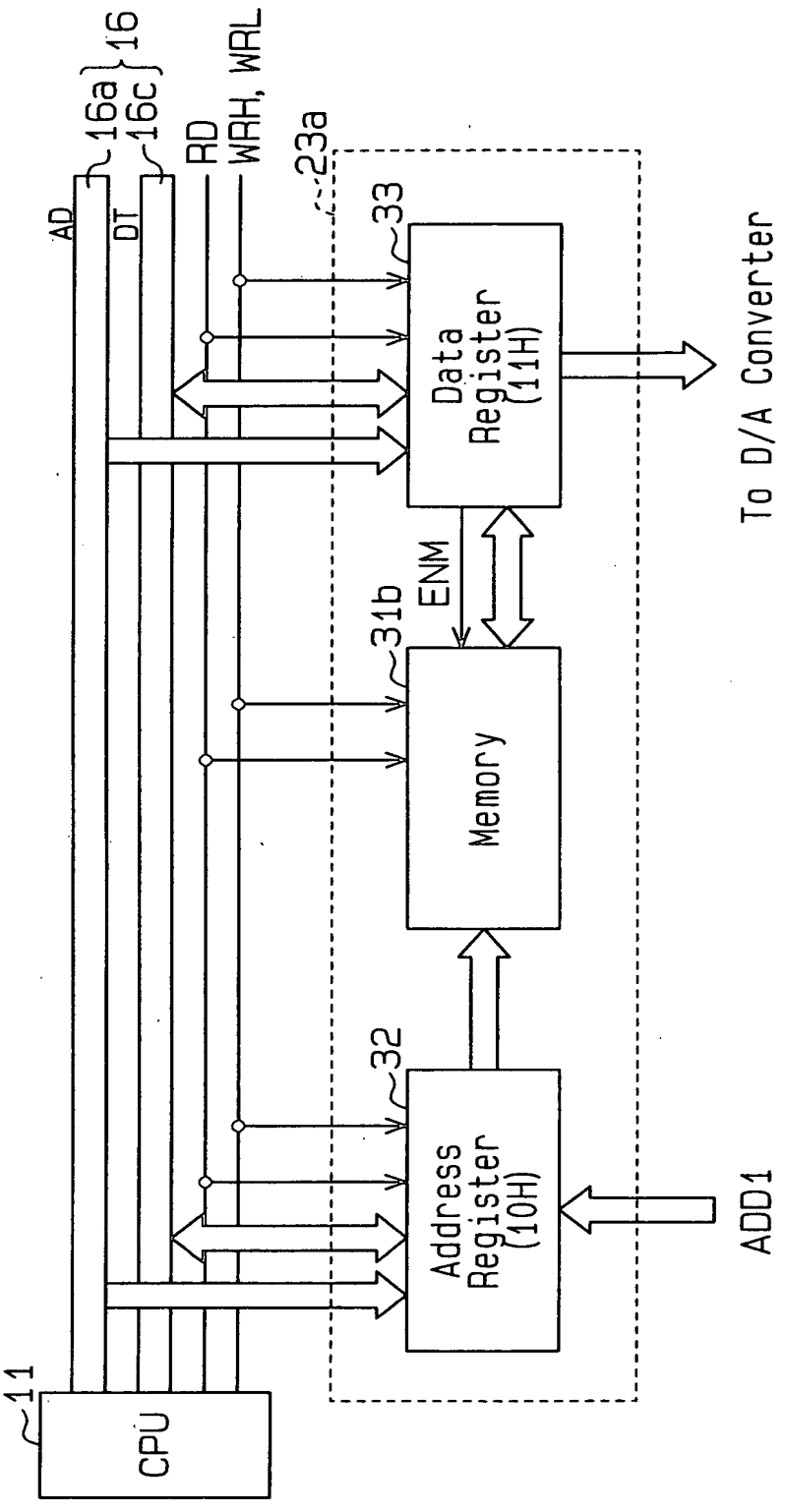

CPU
11
AD
DT
16a
16c
16
RD
WRH, WRL
23a
Address Register (10H)
32
Memory
31b
ENM
Data Register (11H)
33
To D/A Converter
ADD1

Fig.13

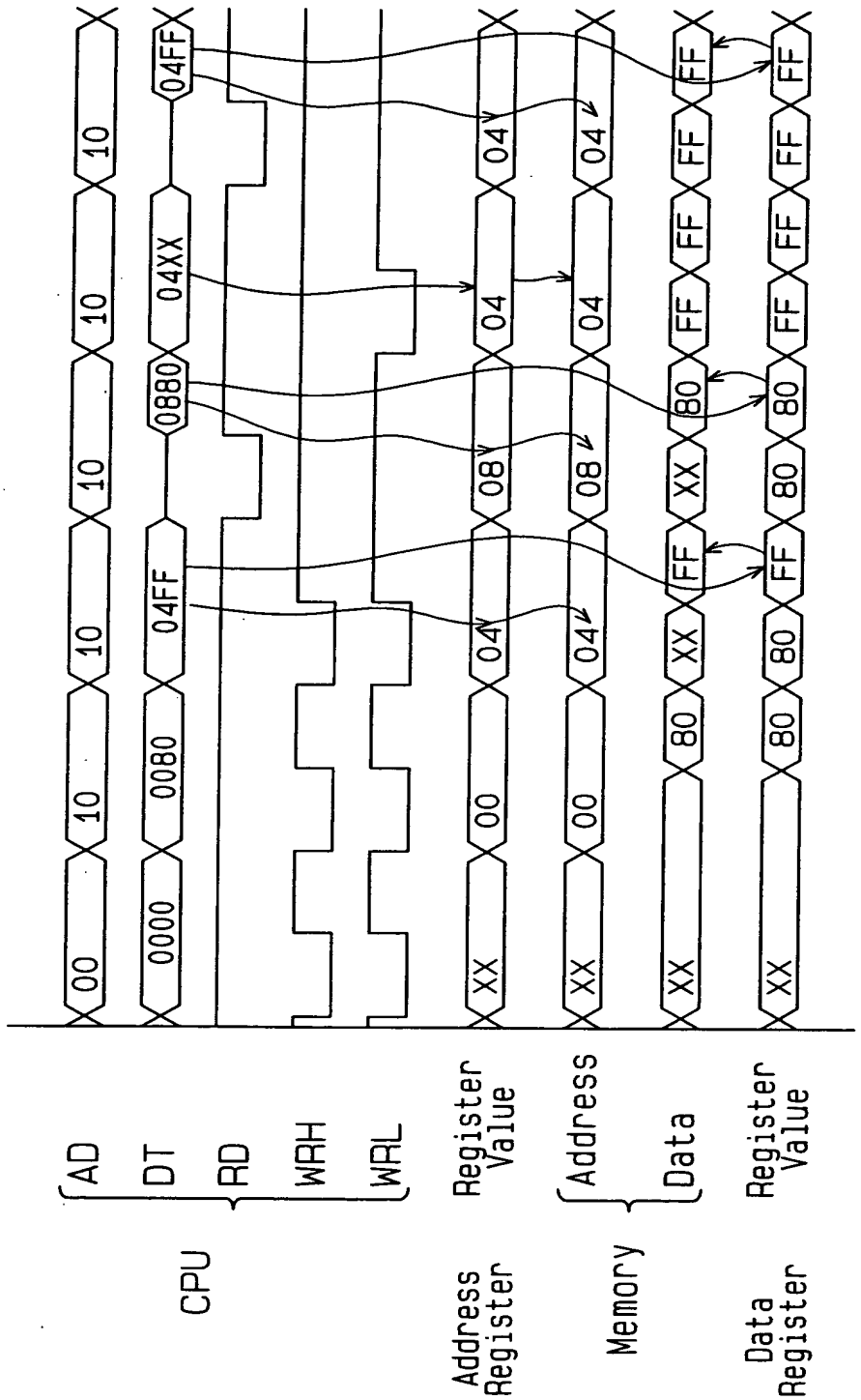

CPU
AD
DT
RD
WRH
WRL
Address Register
Register Value
Memory
Address
Data
Data Register
Register Value
00
10
0000
0080
04FF
0880
04XX
04FF
XX
00
04
08
04
80
FF
XX

Fig.14

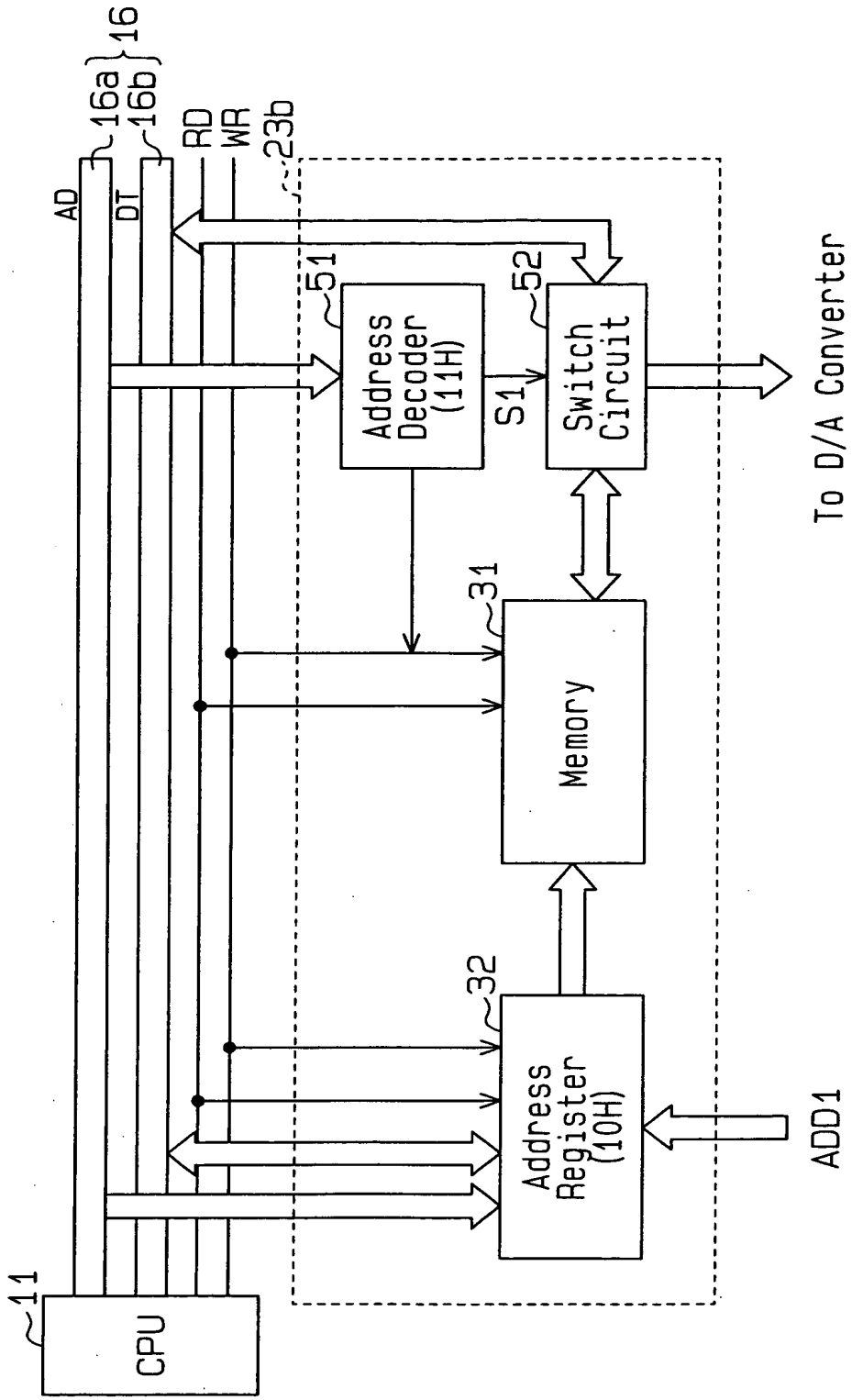

16
16a
16b
AD
DT
RD
WR
23b
51
Address Decoder (11H)
52
Switch Circuit
S1
To D/A Converter
31
Memory
32
Address Register (10H)
ADD1
11
CPU

Fig.15

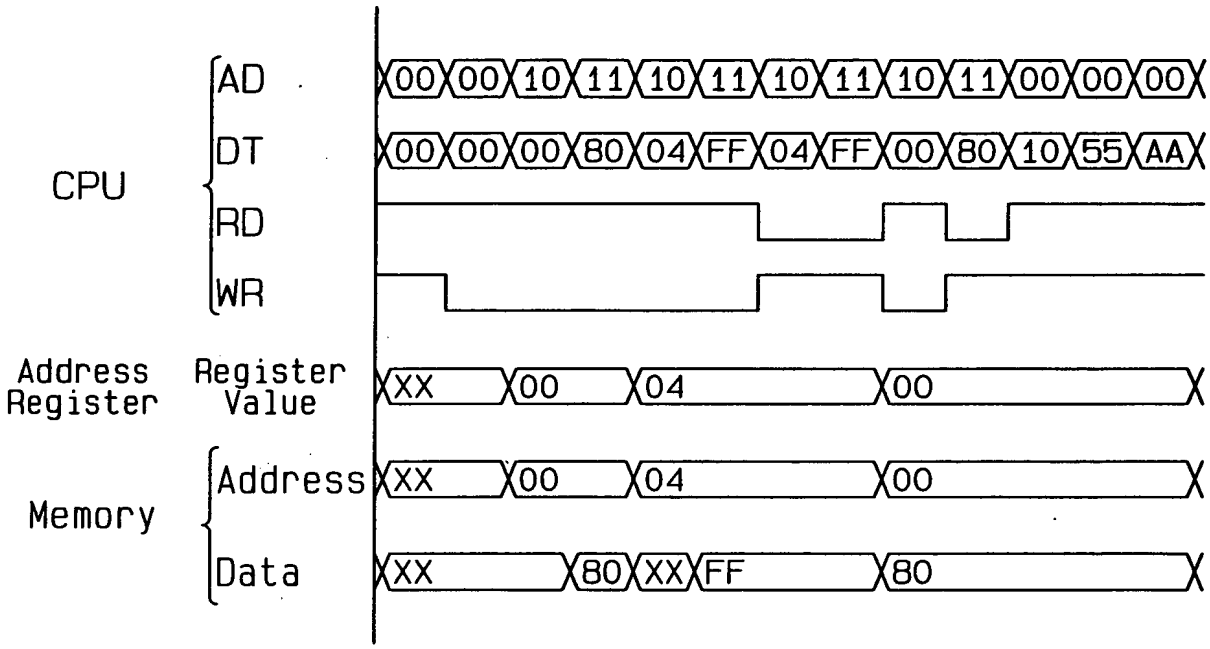

CPU
AD
DT
RD
WR
00 00 10 11 10 11 10 11 10 11 00 00 00
00 00 00 80 04 FF 04 FF 00 80 10 55 AA
Address Register
Register Value
XX 00 04 00
Memory
Address
XX 00 04 00
Data
XX 80 XX FF 80

Fig.16

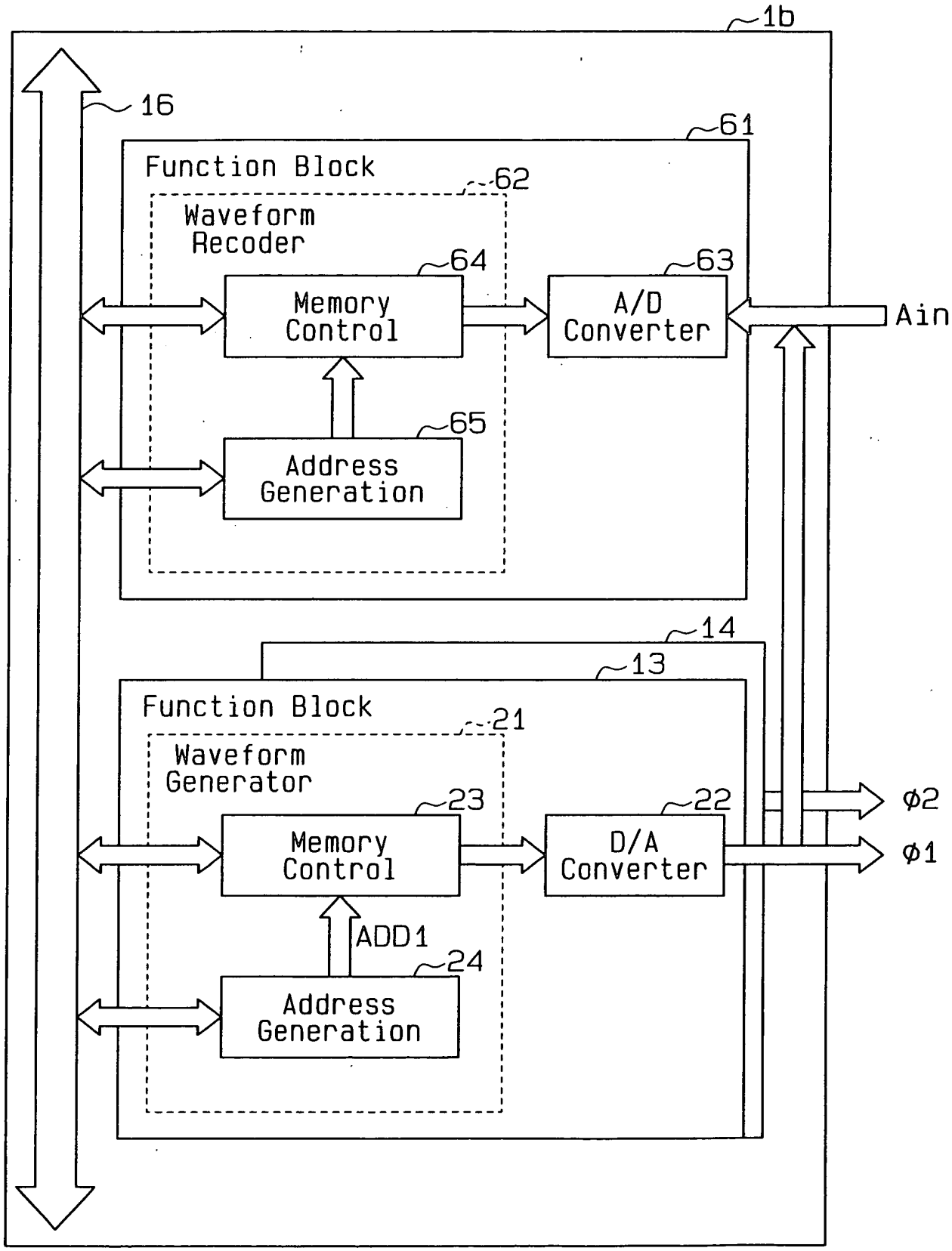
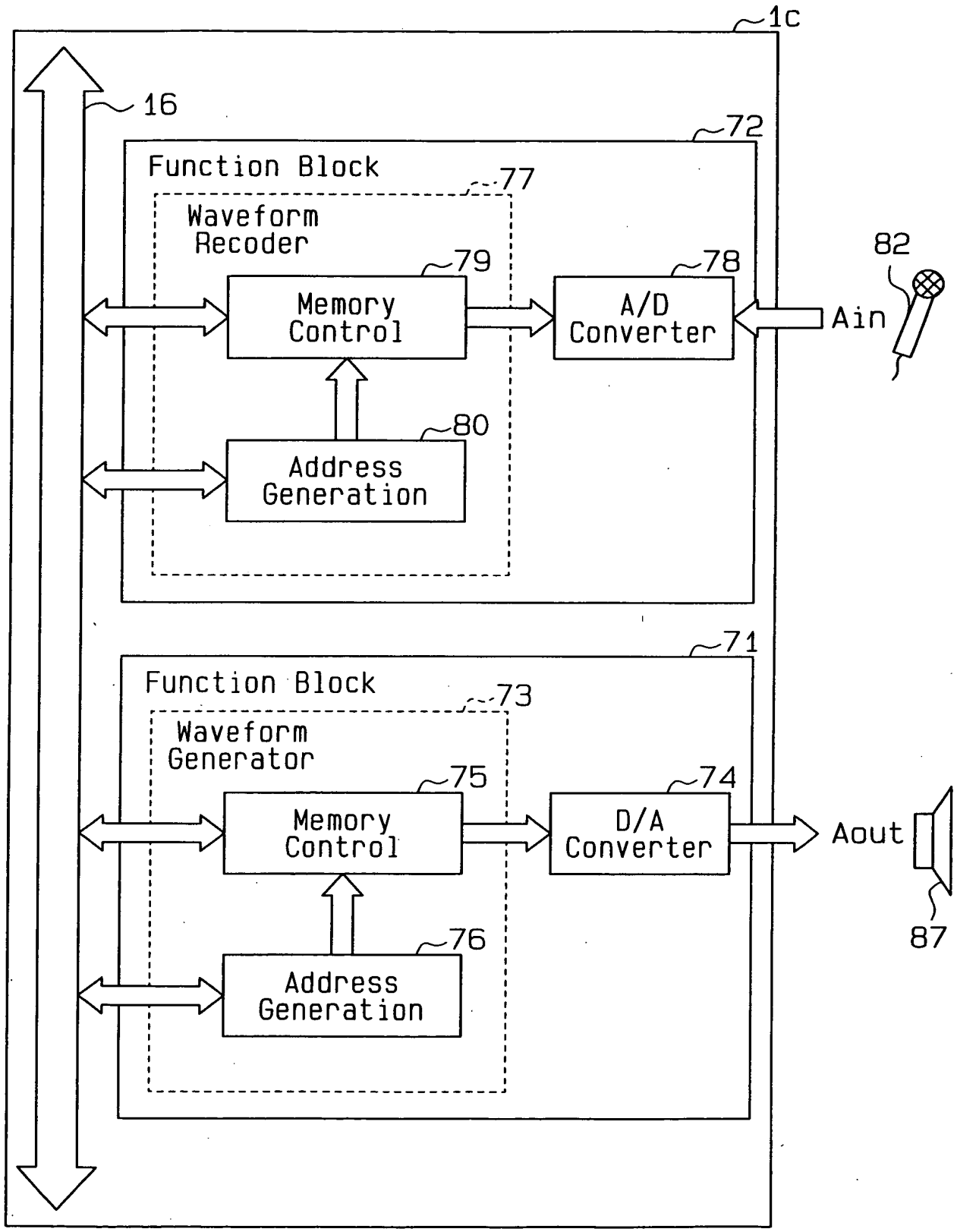

1b
16
61
Function Block
62
Waveform
Recoder
64
Memory
Control
63
A/D
Converter
Ain
65
Address
Generation
14
13
Function Block
21
Waveform
Generator
23
22
Memory
Control
D/A
Converter
φ2
φ1
ADD1
24
Address
Generation

Fig.17


1c
16
72
Function Block
77
Waveform Recoder
79
Memory Control
78
A/D Converter
82
Ain
80
Address Generation
71
Function Block
73
Waveform Generator
75
Memory Control
74
D/A Converter
Aout
87
76
Address Generation